# JC07 Rec'd PCT/PTO 2 2 FEB 2002

FORM PTO-1390 (Modified)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE (REV 11-2000)				ATTORNEY'S DOCKET NUMBER					
(Aur		RANSMITTAL LETTER TO THE UNITED S	STATES	66411-065-2					
		DESIGNATED/ELECTED OFFICE (DO/EO	)/US)	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR					
	CONCERNING A FILING UNDER 35 U.S.C. 371 10/069134								
INTE	RNAT)	TIONAL APPLICATION NO. INTERNATIONAL FILING	DATE	PRIORITY DATE CLAIMED					
CONTRACT E		PCT/F100/00806 9/21/200 NVENTION	0	9/22/1999					
		nvention GE BALANCING IN INTERMEDIATE CIRCUIT O	TAPACITORS						
,	1 <b>8</b> 4 4	III DALIGHOUNG II NAVARANIAN III III III III III III III III II	ALACIACIA						
APPL	APPLICANT(S) FOR DO/EO/US								
Erkki MIETTINEN									
Appli	cant l	herewith submits to the United States Designated/Elected Offi	ice (DO/EO/US) the	e following items and other information:					
1.	$\mathbb{Z}$	This is a FIRST submission of items concerning a filing und	der 35 U.S.C. 371.						
2.		This is a SECOND or SUBSEQUENT submission of items		g under 35 U.S.C. 371.					
3.		This is an express request to begin national examination pro	cedures (35 U.S.C.	371(f)). The submission must include itens (5), (6),					
		(9) and (24) indicated below.  The US has been elected by the expiration of 10 months from	d aniter data						
		The US has been elected by the expiration of 19 months from A copy of the International Application as filed (35 U.S.C. 3		(Article 31).					
THE STATE OF THE S	اليسا	a. Z is attached hereto (required only if not communica		≓					
		b. \(\overline{\sigma}\) has been communicated by the International Burea	·	ional bureau).					
		c. $\square$ is not required, as the application was filed in the U		iving Office (PO/HS)					
		An English language translation of the International Applica		- , ,					
N.		a. $\square$ is attached hereto.							
15		b. $\square$ has been previously submitted under 35 U.S.C. 154	4(d)(4).	,					
		Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))							
		a.   are attached hereto (required only if not communicated by the International Bureau).							
		b.   have been communicated by the International Bure	-	,					
		c. $\square$ have not been made; however, the time limit for materials		nents has NOT expired.					
		d. $\square$ have not been made and will not be made.							
8.		An English language translation of the amendments to the cl		rticle 19 (35 U.S.C. 371(c)(3)).					
9.		An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(							
10.		An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).							
11.		13							
12.	Ø	A copy of the International Search Report (PCT/ISA/210).		ŕ					
		3 to 20 below concern document(s) or information include							
13.		An Information Disclosure Statement under 37 CFR 1.97 and 1.98.							
14.		An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.							
15.		A FIRST preliminary amendment.							
16. 17.		A SECOND or SUBSEQUENT preliminary amendment.							
18.		A substitute specification.  A change of power of attorney and/or address letter							
19.		A change of power of attorney and/or address letter.  A computer-readable form of the sequence listing in accordance with PCT Pule 13ter 2 and 35 U.S.C. 1 921 1 925							
20.		A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.  A second copy of the published international application under 35 U.S.C. 154(d)(4).							
21.		A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).							
22.		Certificate of Mailing by Express Mail							
23.	Other items or information:								
		WO 01/22554; PCT/IB/308; PCT/IB/332; 2 SHEETS OF	FORMAL DRAV	VINGS; PCT REOUEST.					
				,					

JC13 Rec'd PCT/PTO 2 2 FEB 2002

U.S. A	PPLICATION	10/069	134	INTERNATIONAL A PCT/F	APPLICATIO 100/0080		3.			DOCKET NUMBER 1 <b>1-065-2</b>
24.	The fol	lowing fees are subr	mitted:.		· · · · · · · · · · · · · · · · · · ·				CALCULATION	S PTO USE ONLY
	Neither interinterinternational	search fee (37 CFR	y examination (1.445(a)(2))	fee (37 CFR 1.482) r			\$1046	0.00		
	International USPTO but	preliminary examinational Search	nation fee (37 n Report prepa	CFR 1.482) not paid ared by the EPO or JP	to O		\$890	0.00		
:	International	preliminary examin	nation fee (37	CFR 1.482) not paid (2)) paid to USPTO .	to USPTO	)	\$740	0.00		
	International but all claim	preliminary examin s did not satisfy pro	nation fee (37 visions of PC	CFR 1.482) paid to U T Article 33(1)-(4)	JSPTO		\$710	0.00		
	International and all claim	preliminary examinas satisfied provision	nation fee (37 as of PCT Art	CFR 1.482) paid to Uicle 33(1)-(4)	JSPTO ····		\$100	0.00		
		ENTER AP	PROPRI	ATE BASIC FE	EE AMO	DUN	T =		\$1,040.00	
month:	from the ear	<b>0</b> for furnishing the liest claimed priorit	y date (37 CF	ration later than R 1.492 (e)).	□ 20	)	☑ 30		\$130.00	
-	AIMS	NUMBER	FILED	NUMBER EXT	ΓRA		RATE			
Tetal c		2 2	- 20 =	0			\$18.00		\$0.00	
	ndent claims	Claims (check if a	- 3 =	0		X	\$84.00	,	\$0.00 \$0.00	
.C	ie Dependem			ABOVE CALO	CULAT	ION		=	\$1,170.00	
Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.							\$0.00			
112			<del></del>		SUBT	TOT	AL	=	\$1,170.00	
Proces months	sing fee of \$1 from the ear	30.00 for furnishing liest claimed priorit	g the English t y date (37 CF	ranslation later than R 1.492 (f)).	□ 20	)	□ 30	+	\$0.00	
ā		· · · · · · · · · · · · · · · · · · ·		TOTAL NAT	TONAL	FE	E		\$1,170.00	
Fee for accom	recording the	e enclosed assignme appropriate cover sh	ent (37 CFR 1 neet (37 CFR 3	.21(h)). The assignmed 3.28, 3.31) (check if	ent must be	e e).			\$0.00	
N.				TOTAL FEES	ENCL	OSE	D	=	\$1,170.00	
									Amount to be: refunded charged	\$
<del></del> -		1							charged	3
<ul> <li>a.  A check in the amount of to cover the above fees is enclosed.</li> <li>b.  Please charge my Deposit Account No 04-2223 in the amount of \$1,170.00 to cover the above fees. A duplicate copy of this sheet is enclosed.</li> </ul>										
c.	57									
d. Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.										
NOTE 1.137(a	Where an a	appropriate time li at be filed and gran	mit under 37 ted to restore	CFR 1.494 or 1.495 the application to p	has not be ending sta	een m	et, a p	etitio	n to revive (37 CFF	
SEND	ALL CORRE	SPONDENCE TO:			(	$\checkmark$	/	0		
John P. DeLuca Registration No. 25,505 Dykoma Cossett PLI C										
Dykema Gossett PLLC Third Floor West, Franklin Square 1300 I Street, N.W.  John P. DeL					DeLu	ca				
	ngton, DC 2 906-8600	20005-3306		:		25,5		A TIO	N NUMBER	
11	.1.1.11.1.11						ruary			
. 252						DAT	Έ			
		DEMARK OFFIC								

66411-065-2

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	,)	PATENT
Erkki MIETTINEN	į	Group: Unassigned
Serial No. Unassigned	)	Examiner: Unassigned
Filed: Herewith	)	
	)	

# VOLTAGE BALANCING IN INTERMEDIATE CIRCUIT CAPACITORS

# PRELIMINARY AMENDMENT

Washington, D.C. February 22, 2002

Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Prior to examination on the merits, please amend the Application as follows:

### IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) A balancing circuit for voltages of a series connection of capacitors, particularly for intermediate circuit capacitors of an inverter, there being at least two intermediate circuit capacitors connected in series over intermediate circuit voltage, wherein the balancing circuit comprises capacitor-specific freely oscillating inverters, the input poles of which are connected in parallel with the capacitor corresponding to the inverter and the output poles of which are connected in parallel to provide a voltage source (Va).

Please add the following new claim:

2. (New) In an inverter having at least two series connected intermediate circuit capacitors, a balancing circuit comprising:

a freely oscillating inverter for each intermediate circuit capacitor having input poles and output poles, the input poles coupled across the corresponding capacitors and the output poles being connected together in parallel for providing a voltage source.

### **REMARKS**

This Amendment is for the purpose of placing the claim in appropriate U.S. format.

Allowance of the claim is earnestly solicited.

If filing this paper or any accompanying papers necessitates additional fees not otherwise provided for, the undersigned authorizes the Commissioner to deduct such additional fees from Deposit Account No. 04-2223.

Respectfully submitted,

John P. De Luca

Registration No. 25,505

DYKEMA GOSSETT PLLC 1300 I STREET N.W. SUITE 300 W WASHINGTON, D.C. 20005 (202) 906 8600

# VERSION WITH MARKINGS TO SHOW CHANGES MADE

# IN THE CLAIMS:

- 1. (Amended) A balancing circuit for voltages of a series connection of capacitors, particularly for intermediate circuit capacitors [(3)] of an inverter, there being at least two intermediate circuit capacitors connected in series over intermediate circuit voltage, [characterized in that] wherein the balancing circuit comprises capacitor-specific freely oscillating inverters [(4)], the input poles of which are connected in parallel with the capacitor corresponding to the inverter and the output poles of which are connected in parallel to provide a voltage source (Va).
- 2. (New) In an inverter having at least two series connected intermediate circuit capacitors, a balancing circuit comprising:
- a freely oscillating inverter for each intermediate circuit capacitor having input poles and output poles, the input poles coupled across the corresponding capacitors and the output poles being connected together in parallel for providing a voltage source.

10

15

VOLTAGE BALANCING IN INTERMEDIATE CIRCUIT CAPACITORS

# BACKGROUND OF THE INVENTION

The invention relates to a balancing circuit for voltages of a series connection of capacitors, particularly for intermediate circuit capacitors of a frequency converter, there being at least two intermediate circuit capacitors connected in series over intermediate circuit voltage.

Series-connected electrolyte capacitors are usually used as the energy reserve of the DC side in frequency converters. The number of capacitors to be connected in series depends on the supply voltage of the frequency converter, being usually one capacitor for 230 volts, two for 400 to 500 volts, three for 690 volts and four for 1000 volts. Series connections of capacitors can also be connected in parallel in an intermediate circuit. The number of parallel connections depends on the output current of the frequency converter.

The leakage currents of capacitors typically differ from one another, which means that the supply voltage of the static state acting over the series connection is not divided evenly between the capacitors. This may result in a situation where a single capacitor is subjected to a voltage which exceeds the allowed limit in the dynamic state due to the influence of current ripple and capacitance tolerances, for example. For this reason, 'balancing resistors' are usually connected in parallel with the capacitors, the current flowing through the resistors being much higher than the leakage current of the capacitors. In that case the voltage distribution in the static state is mainly determined by the resistance ratios of the resistors. It is also known in the art to use active components in addition to the resistors, e.g. emitter follower connections, which provide stricter restriction without an unreasonable increase in the power loss. However, the use of active components increases the component costs.

Typical balancing resistance for one capacitor in a frequency converter of 100 kVA is 22 kilo ohms, its power dissipation being 5.2 watts with 500 volts, for example. Since with this voltage there are two capacitors and resistors in series, the total power dissipation is 10.4 watts. With higher voltages the power dissipation is naturally even greater.

To operate the frequency converter needs a certain amount of auxiliary power for control circuits and gate drivers. This power is typically 10 to 20 watts in the case of a frequency converter of 100 kVA. It is easy to note that the amount of waste heat produced in the balancing resistors is nearly equal

20

35

5

10

15

20

25

30

to the amount of auxiliary power needed by the whole frequency converter. Thus it would be highly advantageous if the power dissipation required by balancing of capacitors could be utilized as the auxiliary power of the device.

# BRIEF DESCRIPTION OF THE INVENTION

An object of the invention is to provide a circuit which allows to avoid the above-mentioned drawbacks and to balance voltages of a series connection of capacitors in a reliable manner so that an auxiliary voltage source is formed during voltage balancing. This object is achieved with a circuit according to the invention which is characterized in that the balancing circuit comprises capacitor-specific freely oscillating inverters, the input poles of which are connected in parallel with the capacitor corresponding to the inverter and the output poles of which are connected in parallel to provide a voltage source.

The circuit according to the invention is based on the idea that freely oscillating inverter circuits are used for balancing the voltages of series-connected capacitors, the inverter circuits converting voltage supply into voltage to be used in other circuits during voltage balancing. The circuit according to the invention provides the advantage that the power that would otherwise be lost can be utilized in low-power circuits, e.g. as auxiliary voltage in the control circuits and gate drivers of a frequency converter.

# BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in greater detail by means of preferred embodiments with reference to the accompanying drawings, in which

Figure 1 illustrates a balancing circuit for voltages of a series connection of capacitors according to the invention; and

Figures 2 and 3 illustrate inverters used for balancing voltages of capacitors according to the invention.

# DETAILED DESCRIPTION OF THE INVENTION

Figure 1 illustrates a balancing circuit for voltages of a series connection of capacitors according to the invention. The capacitors of Figure 1 are illustrated as capacitors of the intermediate circuit of a frequency converter but the circuit according to the invention can also be utilized in any other applications of the series connection of capacitors. The intermediate circuit of the frequency converter shown in the figure comprises a positive 1 and a negative 2

10

15

20

25

30

35

voltage busbar, between which there are three capacitors 3 connected in series. Figure 1 does not illustrate the actual inverter part of the frequency converter, i.e. power semiconductors and their control circuits because these components are irrelevant to the application and understanding of the invention.

According to the invention, a freely oscillating inverter 4 is connected to the poles of each series-connected capacitor. Examples of freely oscillating inverters are shown in Figures 2 and 3. According to Figure 1, the freely oscillating inverters are connected so that each series-connected capacitor comprises an inverter of its own. Thus the positive pole of each inverter is connected to the positive pole of the respective capacitor and the negative pole to the negative pole of the respective capacitor.

Using the circuit according to the invention the voltage of the electrolyte capacitors functioning as the power reserve of an intermediate circuit in a frequency converter can be balanced so that the auxiliary power needed by the frequency converter is generated at the same time. A freely oscillating inverter formed by two transistors 11, 12 and a converter 13 is connected in parallel with each capacitor, the centre 15 of the primary coil 14 of the converter being connected to the positive pole of the capacitor and the free ends of the same coil to the collectors of the transistors. This kind of embodiment of the invention is shown in Figure 2. Still referring to Figure 2, the emitters of the transistors 11, 12 are connected to the negative pole of the capacitor and the bases as well as a few passive components to the control coil of the converter according to the prior art to form a self-oscillating inverter. The self-oscillating inverter generally refers to the fact that no separate control circuits or timing circuits are used for controlling the semiconductor switches of inverter of this kind. Using passive components it is possible to provide an inverter in which there is no need for separate control power because the semiconductors conduct alternately thanks to oscillation.

In the self-oscillating inverter alternating voltage is induced in the secondary coil 16; 26 of the converter 13;23, which is rectified with a rectifying bridge 17; 27 to provide a direct current that can be used as the auxiliary voltage. The full-wave rectified outputs of all inverters are connected together as shown in Figure 1 to provide an intermediate voltage Va, e.g. 24 V  $\pm$  30%, which is suitable for supply of auxiliary power. The number of turns of the secondary coil of the converters in the inverters is adjusted with respect to the

primary coil so that this voltage is achieved with a typical terminal voltage of the energy reserve capacitor. It is clear that large tolerances should be allowed for this intermediate auxiliary voltage because the range of variation of the primary voltage is also large.

5

Depending on the inverter solution used, the transistors of the inverter should withstand a voltage which is 1.2 or 2 times the capacitor voltage, which in the worst case, i.e. with a mains voltage of 500 volts and an overvoltage of 30%, is 878 volts. Thus it is possible to select transistors intended for a collector voltage of 1000 volts, in which case the inverter circuit is at its simplest (Figure 2), or transistors of 600 volts, in which case a few additional components are needed for the circuit (Figure 3).

10

15

The output and input voltages of the inverter circuit shown follow each other when multiplied by the transformation ratio of the converter, i.e. if the input voltage increases, rectified output voltage also increases accordingly. The influence of any unideal properties of the inverter on this dependency is typically very small.

1 1 20 Since the rectified outputs of the converters are connected together as shown above so that they retain their polarity, the auxiliary voltage power flows mainly through the converter with the higher secondary voltage. This means that most of the auxiliary voltage power is taken from the energy reserve capacitor the terminal voltage of which tends to be the highest with respect to the other series-connected capacitors. Thus energy flows out of the capacitor, which means that the terminal voltage of the capacitor decreases until it reaches the second highest terminal voltage. However, this interaction occurs simultaneously between all capacitors, and consequently the terminal voltages will be equal and the supply of auxiliary power is divided almost evenly between the inverters.

30

25

This solution provides active balancing of energy reserve capacitors with virtually no loss of power, while the circuit can be used for supplying auxiliary voltage, e.g. in connection with a frequency converter.

35

An additional advantage of the invention is that the components of the inverters are not dependent on the mains voltage. In all cases the number of series-connected inverters comprising the same components increases along with the input voltage, and thus expensive high-voltage switch components are not needed even with high supply voltages, which is the case in solutions based on separate auxiliary current sources driven directly by the in-

10

15

20

termediate circuit voltage. If the supply voltage is around 1000 volts, standard switch components are not even available.

The output power of frequency converters tends to be higher when the supply voltage is high. In that case one needs more auxiliary power because the number of gate drivers is larger, but thanks to several series-connected intermediate circuit capacitors, a corresponding number of inverters the secondary circuits of which are connected in parallel are available for this purpose.

The inverter and its secondary rectifier used in the circuit according to the invention can be implemented easily using a piece of a circuit board, or as a unit cast in epoxy, which, being a low-loss unit, is easy to connect directly to the poles of a power capacitor. The price of such a volume component can be reduced considerably, and, if necessary, the converters can be provided with reinforced insulation, in which case the intermediate voltage of the auxiliary power can be rendered to the earth potential to enable parallel battery use when the intermediate circuit voltage has not been switched on or it is too low with respect to the normal operation. It is also easy to implement a blocking circuit for accidental start-up in the earth potential.

It is obvious to a person skilled in the art that the inventive concept can be implemented in various ways. The invention and its embodiments are thus not limited to the examples described above, but they may vary within the scope of the claims. A balancing circuit for voltages of a series connection of capacitors, particularly for intermediate circuit capacitors (3) of an inverter, there being at least two intermediate circuit capacitors connected in series over intermediate circuit voltage, **characterized** in that the balancing circuit comprises capacitor-specific freely oscillating inverters (4), the input poles of which are connected in parallel with the capacitor corresponding to the inverter and the output poles of which are connected in parallel to provide a voltage source (Va).

10

5

### (19) World Intellectual Property Organization International Bureau



#### (43) International Publication Date 29 March 2001 (29.03.2001)

## PCT

# (10) International Publication Number WO 01/22554 A1

CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC,

(51) International Patent Classification7: H02M 5/40

H02J 7/00.

(74) Agent: KOLSTER OY AB; Iso Roobertinkatu 23, P.O. Box 148, FIN-00121 Helsinki (FI).

(21) International Application Number:

PCT/FI00/00806

(81) Designated States (national): JP, US.

(22) International Filing Date:

21 September 2000 (21.09.2000)

(84) Designated States (regional): European patent (AT, BE,

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

19992031

22 September 1999 (22.09.1999)

Published:

With international search report.

Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of

amendments.

NL, PT, SE).

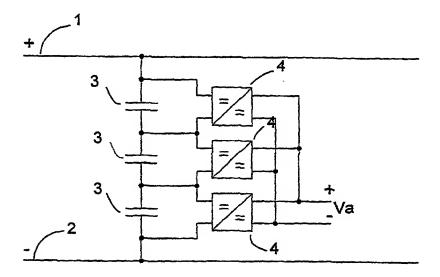
(71) Applicant (for all designated States except US): ABB IN-DUSTRY OY [FI/FI]; Hiomotie 13, FIN-00380 Helsinki **(FI)**.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(72) Inventor; and

(75) Inventor/Applicant (for US only): MIETTINEN, Erkki [FI/FI]; Kirkkokatu 1 b A 1, FIN-00170 Helsinki (FI).

(54) Title: VOLTAGE BALANCING IN INTERMEDIATE CIRCUIT CAPACITORS



(57) Abstract: A balancing circuit for voltages of a series connection of capacitors, particularly for intermediate circuit capacitors (3) of an inverter, there being at least two intermediate circuit capacitors connected in series over intermediate circuit voltage. The balancing circuit comprises capacitor-specific freely oscillating inverters (4), the input poles of which are connected in parallel with the capacitor corresponding to the inverter and the output poles of which are connected in parallel to provide a voltage source (Va).

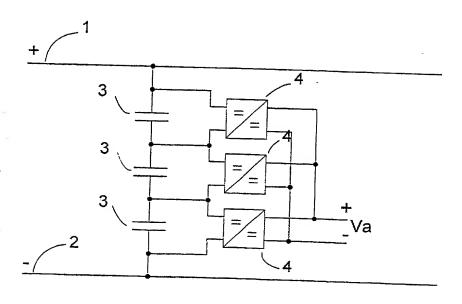


FIG. 1

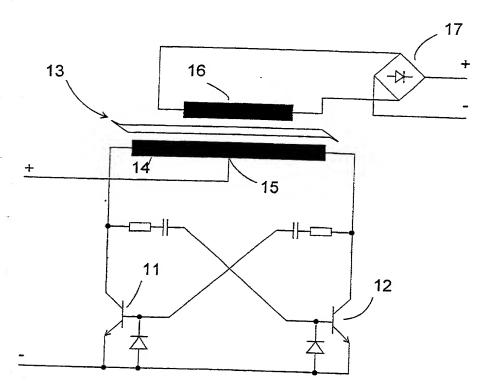


FIG. 2

2/2

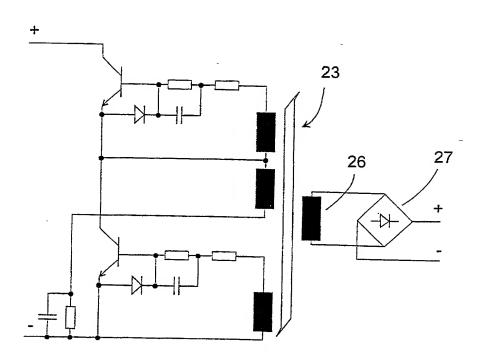


FIG. 3

# COMBINED DECLARATION AND POWER OF ATTORNEY FOR UTILITY PATENT APPLICATION (Includes PCT)

Attorney Docket No.

As a below named inventor, I hereby declare that:

Application No.

My residence, post office address and citizenship are as stated below next to my name;

that I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are listed below) of the subject matter which is claimed and for which a Patent is sought on the invention entitled:

**VOLTAGE BALANCING IN INTERMEDIATE CIRCUIT CAPACITORS** 

Day/Month/Year Filed

	the specification of which (check one):							
	[ ]	is attached hereto						
•		was filed on ended on	as Ap	olication Serial No		and was		
V	on on	21 September 2000		ler PCT Article 19 on				
	hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.							
	facknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, '1.56(a).							
	America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application.							
I hereby claim foreign priority benefits under Title 35, United States Code '119 of any foreign application(s) fe patent or inventor's certificate listed below and have also identified below any foreign application for patent inventor's certificate having a filing date before that of the application(s) on which priority is claimed:								
	Prior Forei	gn Application(s)			Prio	rity Claimed		
	19992031 (Number)	<u> </u>	Finland (Country)	22 September 1999 Day/Month/Year Filed	[x] Yes	[] No		
	(Number)		(Country)	Day/Month/Year Filed	[] Yes	[ ] s No		
	(Number)		(Country)	Day/Month/Year Filed	[ ] Yes	[] No		
	I hereby of application	laim the benefit เ เ(s) listed below:	ınder Title 35, United	States Code, '119 (e)	of any United Stat	es provisional		
	Application	1 No.	Day/Month/Year Filed					

I hereby claim the benefit under Title 35, United States Code, '120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, '112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, '1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Attorney Docket No. \_\_\_\_\_

Application Serial No.	Filing Date	Status (patented, pendin	g, abandoned)				
Application Serial No.	pplication Serial No. Filing Date Status (patented, pending, abandoned)						
I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Lawrence R. Radanovic, Reg. No. 23,077; Richard H. Tushin, Reg. No. 27,297; Donald N. Huff, Reg. No. 27,561; John P. DeLuca, Reg. No. 25,505; Michael Regman, Reg. No. 42,318; Sandra S. Snapp, Reg. No. 41,444; Charles Rutherford, Reg. No. 18,933; Robert L. Kelly, Reg. No. 31,843; Kevin M. Hinman, Reg. No. 35,193; Ernest E. Helms, Reg. No. 29,721; William F. Kotakowski, Reg. No. 41,908; and John F. Buckert, Reg. No. 44,572, all of Dykema Gossett PLLC. Direct all telephone calls to telephone no. (202) 522-8600 and faxes to (202) 522-8669.  Address all correspondence to Dykema Gossett PLLC, Suite 300 West, 1300 I Street, N.W., Washington, D.C. 2005-3306.  I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.							
Full Name of First Joint In	ventor	Inventor's Signature	Date				
Erkki MIETTINEN		Pakhi for					
Residence:	ki, Finland	FIX	Citizenship <u>Finnish</u>				
Post Office Address:							
Kirkkol	katu lb Al, FIN-	00170 HELSINKI, Finland					
Full Name of Second Join	t-Inventor	Inventor's Signature	Date				
Residence:  Post Office Address:			Citizenship				
Full Name of Third Joint I	nventor	Inventor's Signature	Date				
Residence:—			Citizenship				

100